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Design and Simulation of an Operational Amplifier with High Gain and Bandwidth for Switched Capacitor Filters

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Abstract: *Operational amplifiers can be found in buffer, adder, comparator, negative impedance converter, and integrator and differentiator circuits. In fact, operational amplifiers are basic blocks of analog and digital circuits. In this article, a single-stage operational amplifier with CMOS 180nm technology was designed. The amplifier was simulated with the help of HSPICE. Gain Boosting (GB) technique was used to increase the amplifier gain. The simulation results showed an increase of 88% in the gain after applying GB technique. The amplifier bandwidth was about 1.17 GHz which was much higher than amplifiers with the same gain. A high-pass filter with a cutoff frequency of 3 dB-10 MHz was designed using the proposed amplifier.*
Keywords: *Operational amplifier, swing, switched capacitor filter, Gain Boosting technique*

I. Introduction

High gain and bandwidth amplifiers are required in integrated analog circuits such as switched capacitor filters, Delta Sigma modulators, and analog-to-digital converters to guarantee the accuracy and speed of the system. The speed and accuracy of an amplifier are characterized by its large signal behavior. Fast settling time means a high unit gain frequency. On the other hand, accuracy is achieved with a high DC gain [1]. Realization of amplifier structures is a practical challenge and needs a compromise between gain, bandwidth, swing, etc. Different structures, each with several advantages and disadvantages, have been proposed for amplifiers. Due to intrinsic low gain of short channel transistors, it is difficult to achieve a high gain using conventional topologies [1]. To overcome this problem, the proposed methods are applied on the main body of amplifiers to improve specifications [2, 3]. Gain Boosting (GB) technique is one of the methods to increase the gain. This technique improves DC gain of an amplifier without affecting the speed by adding a sub-circuit in the output stage cascode transistors. Accordingly, the amplifier gain is improved by increasing the output impedance. In this method, high-frequency behavior of a single-stage amplifier is combined with the high-gain of a multistage amplifier [4]. The aim of the present study is to design a high gain and bandwidth amplifier to be used in a switched capacitor filter. Various types of amplifiers are discussed in Section 2. In the third section, the design method and GB technique used in this topology and the structure of switched capacitor filter are discussed. Simulation results are presented in Section 4. The conclusions are presented in the last section.

II. Theoretical Background

Generally, a transistor with a load on its output can be used as an amplifier. However, different applications require amplifiers with different specifications. Depending on the application, gain, bandwidth, power consumption, swing and other parameters become more important. Thus, various structures have been proposed as basic topologies in the design of amplifiers [5]. The simplest type of amplifier is shown in Figure 1. This structure is known as the fastest amplifier with maximum bandwidth and minimum gain [5]. The gain for this amplifier is calculated from equation (1) [5].

$$A_v = g_{mN} \times R_{out} = g_{mN} \times (r_{ON} || r_{OP}) \quad (1)$$

where A_v is gain, g_{mn} transistor transconductance, and R_{out} is output resistance. Because of low number of output transistors, this structure will have a maximum swing. Swing in this structure is calculated from:

$$Swing = 2 \times \left(V_{DD} - V_{od,n1} - V_{od,ss} - \left|V_{od,p1}\right|\right) \quad (2)$$

where V_{DD} is DC voltage of amplifier and $V_{od,n1}$, $V_{od,p1}$, $V_{od,ss}$ are effective voltages of transistors n1, p1, and the current source, respectively.

This structure is not suitable for common applications and needs some modifications. The first solution is to use series of transistors in the output. This structure is known as cascode structure. Cascode transistors increase output resistance and significantly improve the amplifier gain [5].

In this structure, gain significantly increases. However, bandwidth is much reduced as compared with the single-stage structure because of smaller dominant pole. Cascode amplifiers are fast, but swing is significantly reduced because of adding transistors to increase the output impedance. Accordingly, they are not suitable in applications with low supply voltage. So, the main disadvantage of this structure is limited swing [5].

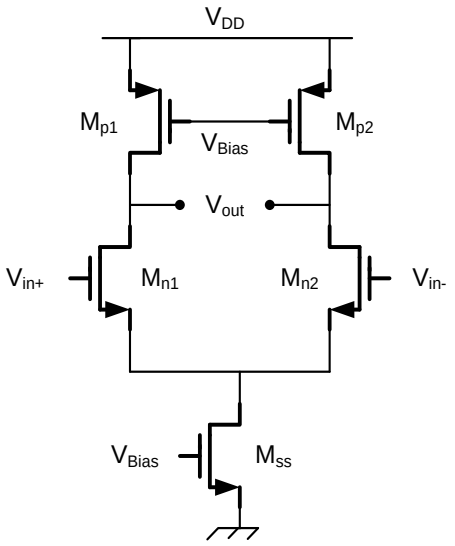

Figure 1: Single-stage amplifier

To increase the swing of cascade structure, folded cascode structure has been proposed [5]. In this method, by eliminating the transistor of cascode sequence, the number of cascode transistors in the output is reduced and thus swing increases by the effective voltage of a transistor [4]. By folding the output stage, cascode transistors are not located on input transistors. As a result, the input voltage range is larger than that in cascode structure. This structure can be used with low voltage sources in the case where the output voltage has a high swing. In addition, the input and output common mode levels can be equally adjusted. The voltage gain of this structure is less than cascode amplifier. Folded cascode amplifiers are slower than telescopic amplifiers. Despite their many advantages, folded cascode amplifiers suffer from higher power losses, lower voltage gains and more noises [6].

However, in cases where a higher swing is required, this structure is the first choice and is widely used for the same reason [6].

Increasing gain in single-stage operational amplifiers will reduce the output voltage range. To solve this problem, a two-stage topology can be used in which the first stage increases the gain and the second stage increases the range of output voltage. Increasing the number of stages increases the gain and at the same time leads to a complicated circuit with a lower speed [7].

Thus, multistage structures must be used to achieve a high gain. Multistage amplifiers are fast, but have a complicated circuit structure with much more power consumption. Table 1 compares the amplifiers presented in this section [5].

The structure of an amplifier is selected based on objective requirements in accordance with Table 1. For switched capacitor filters with high bandwidths, cascode or folded cascode amplifier can be used. Single-stage structure is not suitable due to very low gain. Despite the high gain of two-stage structure, it is unable to provide the required bandwidth [8].

Table 1: Comparison of amplifiers with different structures

Structure	Swing	Bandwidth	Gain
Single-stage	Very high	Very high	Low
Cascode	Low	Moderate	High
Folded cascode	Moderate	High	Moderate
Two-stage	Very high	Low	Very high

III. Amplifier Design

According to Second II, the optimal structure was to be selected first. For a switched capacitor filter, an amplifier with high gain and bandwidth is desirable. On the other hand, the system speed should also be acceptable. As a result, a structure with a proper settling time should be designed. All these requirements cannot be satisfied. However, a compromise must be made between the above parameters. The differential structure is a very good choice due to its unique characteristics [9].

3.1. Folded Cascode Amplifier

This amplifier has a moderate gain and bandwidth. But in low voltage applications, it is preferred to use this structure because of high swing. On the other hand, the input dynamic range in this structure is larger. Power loss is one of disadvantages of this structure. To decrease power loss, the branches connected to the source are located on the bottom. As a result, the dominant pole is closer to the source and therefore the bandwidth will be affected [10]. Figure 2 shows the optimal structure of amplifier.

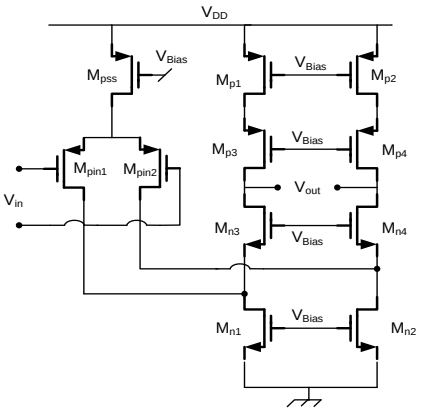

Figure 2: Folded cascode amplifier [3]

3-2. Gain Boosting (GB) technique

In new technologies, the inherent declining gain of the amplifier due to channel length reduction causes restrictions when high-gain amplifiers are designed. Certainly a folded cascode stage will not have a proper gain to be used in a filter. Low gain will lead to a gain error. Increasing the gain by adding a second stage will increase the power loss. By adding a second pole, the overall bandwidth of the system will distort. The same factors provide the ground for research on structures with low cost and high efficiency. One of these structures is GB technique. The main idea of this technique is shown in Figure 3 [10].

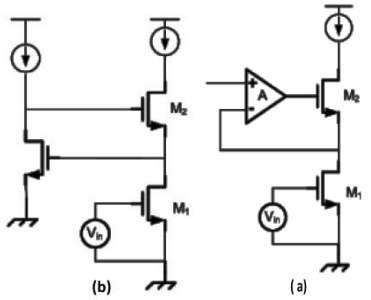

Figure 3: The main idea of Gain Boosting technique, (a) the block diagram, (b) circuit structure [10]

Adding a second stage with a gain of A increases the output resistance. The output resistance of GB is obtained from equation (3) [10].

$$R_0 = A.g_{m2}r_{o1}r_{o2} \quad (3)$$

where A_0 is open loop gain of the amplifier block, r_{o1} and r_{o2} are respectively output resistances of input transistor and cascode and g_{m2} is transconductance of cascode transistor. A transistor can be used instead of an amplifier block. In this case, A will be the gain of transistor. The resistance of the structure shown in Fig. 3 (b) is calculated from equation (4).

$$R_0 = G_m R_0 g_{m2} r_{o1} r_{o2} \quad (4)$$

where $G_m R_O$ is the gain of additional stage. Taking into account the GB stage, the gain of folded cascode amplifier can be obtained from equation (5)

$$A_v = g_{mpin}\left[g_{mA7}(r_{oA7}||r_{oA5})(g_{mn3}+g_{mnb3})r_{on3}(r_{on1}||r_{opin})\right]||\left[g_{mA3}(r_{oA3}||r_{oA1})(g_{mp3}+g_{mpb3})r_{op1}r_{op3}\right] \quad (5)$$

where G_m is transconductance of transistors and r_o is observed resistance of the output transistors. Figure 4 shows the final structure of the proposed folded cascode amplifier with GB stage.

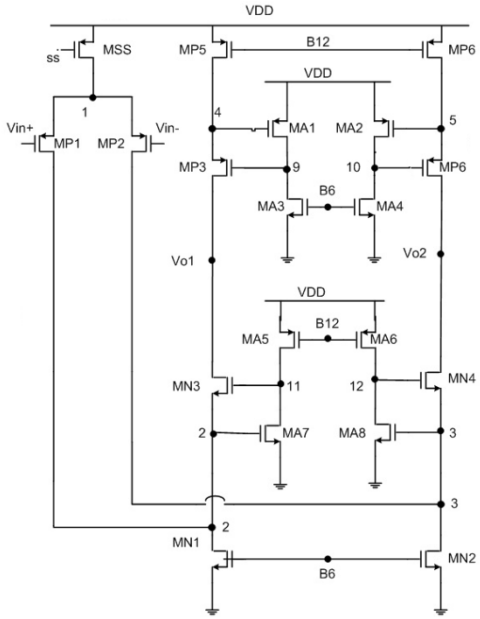

Figure 4: The proposed amplifier

IV. Switched Capacitor Filter

Operational amplifiers are mainly used to design switched capacitor filters. The filters are obtained by replacing a resistance with a capacitor and two stringent switches [5]. Figure 5 shows a filter designed using the amplifier. This is a high-pass filter of the first order with a cutoff frequency of 3 dB-10 MHz

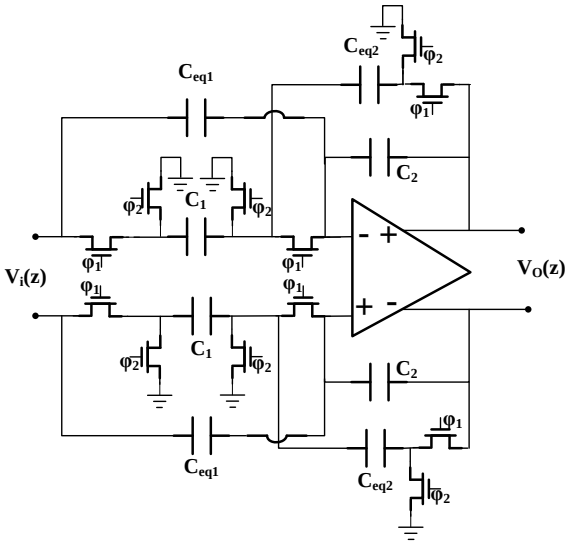

Figure 5: Differential first-order high-pass filter [11]and a sampling frequency of 100 MHz. According to Niquest criterion, the input signal frequency is considered to be less than half the sampling frequency, i.e. less than 50 MHz [11].

V. Simulation

The proposed amplifier with CMOS 180nm technology was simulated in HSPICE. Figure 6 shows the frequency response of the amplifier. As can be seen, DC amplifier gain is about 76 dB. This shows an increase of 88% compared with the frequency response of the folded cascode amplifier (Figure 7). With a significant increase in gain, reduction in unit gain bandwidth is quite obvious. Figure 6 shows a bandwidth of 1.17 GHz for the amplifier which is well suited for the intended use. In addition, the phase margin is close to 77 degrees indicating the stability and proper linearity of the proposed structure.

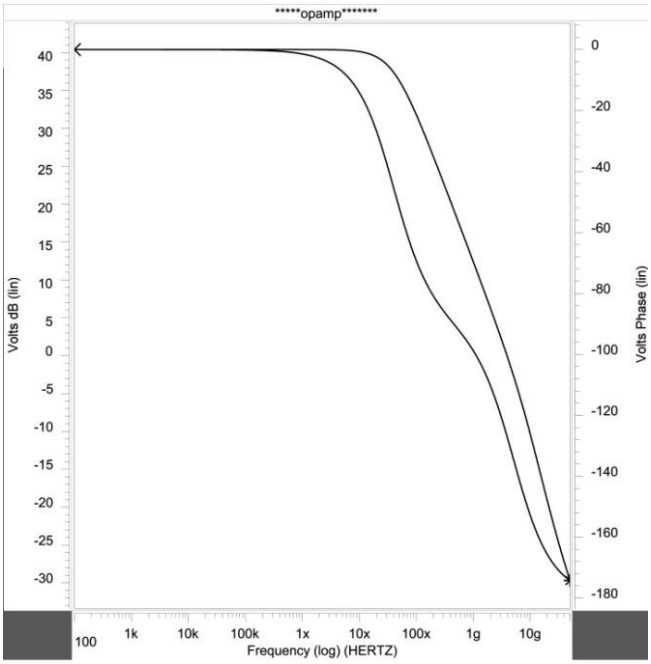

Figure 6: Frequency response of the folded Cascode amplifier

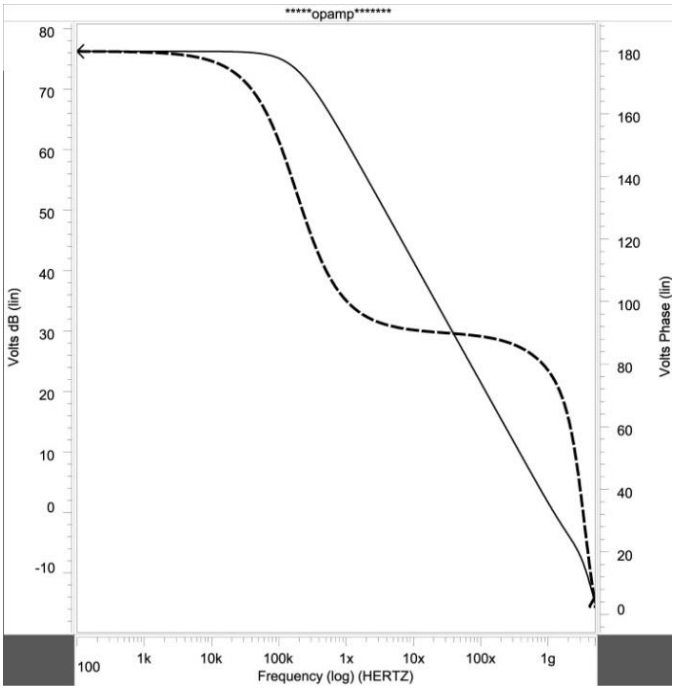

Figure 7: Frequency response of the proposed amplifier

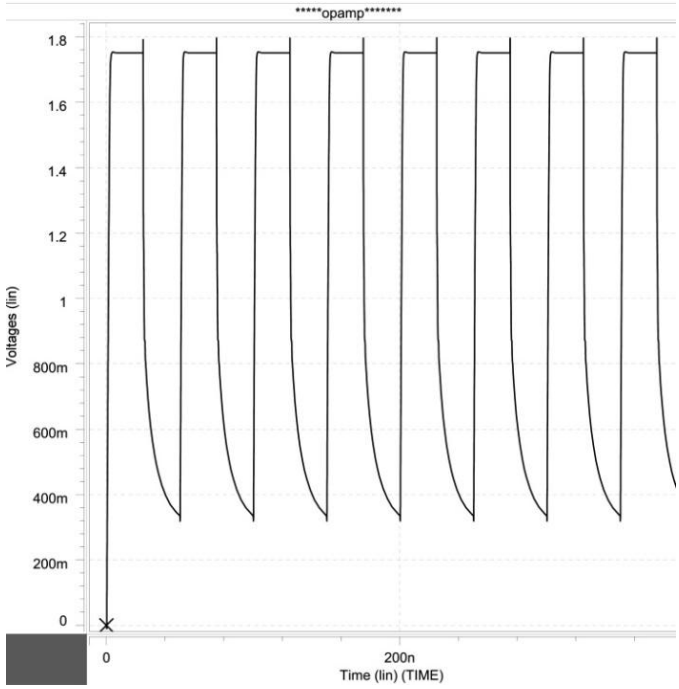

Figure 8: Amplifier response to step input

To calculate settling time, spin rate, and speed, amplifier response to a step input is used. Figure 8 shows the amplifier response to a step input. As can be seen, the settling time for the rising edge is lower than the falling edge. The spin rate indicates an acceptable speed of the proposed amplifier. Table 2 compares the results. As shown, the power loss of the proposed amplifier is significantly lower than similar amplifiers. The spin rate is also acceptable. In addition, increased gain decreases bandwidth and this remains as a design challenge.

Table 2: Comparing the proposed amplifier with other similar amplifiers

Specifications	[11]	[9]	[7]	Proposed amplifier
Technology (nm)	180	180	180	180
DC gain (dB)	110	84	68.48	76
Unit gain bandwidth (MHz)	821	45.12	247.1	1170
Phase margin (degrees)	70	81	26.3	77
Power loss (mW)	7.8	9	92.49	1.55
Settling time (nS)	3.7	85	12.39	11
Spin rate (V/us)	35	97	92.8	100

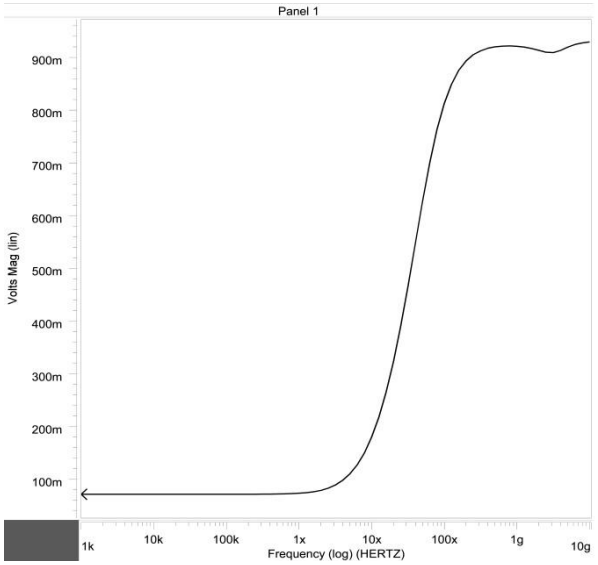

Figure 9: Output of high-pass filter designed with the proposed amplifier

To ensure proper functioning in the proposed amplifier, the amplifier was used along with a high-pass filter in Figure 5 and simulated by HSPISE. Figure 9 shows the first-order high-pass filter output. As can be seen, this structure filters out low frequencies and passes high frequencies. However, there is a small error in the output caused by nonlinear factors in circuit elements.

VI. Conclusion

A single-stage amplifier with high gain and bandwidth was designed and simulated for subsequent use in switched capacitor filters. Gain Boosting (GB) technique was used to achieve a high gain in the single-stage structure. A large phase margin was considered to increase stability of the amplifier. According to the simulation results, gain was reasonably increased. Despite a reduction as compared with the original structure, the bandwidth was also reasonable. A large-signal response was used to calculate the settling time for the rising and falling edges. According to the relevant definitions, the slope of the resulting line was considered as spin rate. The spin rate was also acceptable due to the fast rising edge in the proposed structure. Despite the advantages described for the proposed structure, the settling time of the falling edge is lower than the rising edge and this drawback must be eliminated in future studies.

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